planar surface formed parallel to and near the plane of tips of the plurality of emitters.

The porous dielectric results in the emitter conductors having reduced capacitance C compared to prior art dielectric layers. Charging and discharging of the emitter conductors in order to drive the emitters forms a major component of the electrical power consumed by the display. By reducing the capacitance of the emitter conductors, the display is able to form luminous images, such as text and the like, while dissipating reduced electrical power.

In another aspect of the present invention, tips of the emitters are formed from a material having a work function less than four electron volts. The voltage needed in order to drive the emitters, and hence the voltage used to charge and discharge the columns, is proportional to a turn-on voltage for the emitters. Emitters having reduced turn-on voltage draw less electrical power. As a result, baseplates with emitters having low work function tips are able to form luminous images while dissipating reduced electrical power compared to conventional displays.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a simplified side cross-sectional view of a portion of a display including a faceplate and a baseplate, in accordance with the prior art.

Figure 2 is a simplified plan view showing rows and columns of the emitters of Figure 1, in accordance with the prior art.

Figure 3 is a simplified flowchart of a process for forming a dielectric having a reduced relative dielectric constant ε_R, in accordance with embodiments of the present invention.

Figure 4 is a simplified side view of an emitter having a body formed of high resistivity material and a tip formed of a low work function material, in accordance with embodiments of the present invention.

Figure 5 is a simplified flowchart of a process for forming emitters having reduced work function and integral ballast resistors, in accordance with embodiments of the present invention.

Figures 6A-6G show the baseplate at various stages in the process of emitter formation, in accordance with embodiments of the present invention.

Figure 7 is a simplified block diagram of a computer including a field emission display, in accordance with embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 3 is a simplified flowchart of a process 75 for forming a dielectric layer 34' (not shown in Figure 3) having a reduced relative dielectric constant ε_R, relative to the prior art, in accordance with embodiments of the present invention. The process 75 begins with a step 77 of forming emitter conductors defining columns 44 (Figure 2) on the substrate 32 (Figure 1). In a step 79, a silicon layer (not shown) is formed on the substrate 32 and on the emitter conductors/columns 44 by conventional processes. In one embodiment, the step 79 includes forming the silicon layer by conventional deposition of polysilicon.

In a step 81, the silicon layer is made porous. In one embodiment, the step 81 includes forming voids or pores (not shown) in an n-type silicon layer by a process similar to that described in "Formation Mechanism of Porous Silicon Layers Obtained by Anodization of Monocrystalline n-type Silicon in HF Solutions" by V. Dubin, Surface Science 274 (1992), pp. 82-92. In one embodiment, a current density of between 5 and 40 mA/cm^2 is employed together with 12-24% HF. In general, increasing N_D (silicon donor concentration), HF concentration or anodization current density provides larger pores.

In another embodiment, the step 81 includes forming voids or pores in a p-type silicon layer by a process similar to that described in "On the Morphology of Porous Silicon Layers Obtained by Electrochemical Method" by